



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,617	05/20/2004	Adam William Saxler	5308-413	9882
20792	7590	04/20/2006	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC				DUONG, KHANH B
PO BOX 37428				
RALEIGH, NC 27627				
		ART UNIT		PAPER NUMBER
		2822		

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/849,617	SAXLER ET AL.	
	Examiner	Art Unit	
	Khanh B. Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 17 November 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-45 and 63-80 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-8,13-21,23-45 and 63-80 is/are rejected.
 7) Claim(s) 9-12 and 22 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II, claims 1-45 and 63-80 in the reply filed on November 17, 2005 is acknowledged.

Accordingly, the non-elected claims 46-62 and 81-84 were canceled.

Currently, claims 1-45 and 63-80 remain pending.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 8/26/2004, 8/30/2004, 10/26/2004, 1/27/2005, 6/16/2005, 7/5/2005 and 7/13/2005 are being considered by the examiner.

Specification

The disclosure is objected to because of the following informalities: page 19, line 12, after "sidewall", "spaces" should be --spacers--, and line 14, after "to", "provided" should be --provide--.

Appropriate correction is required.

Claim Objections

Claim 36 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 17. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim 43 is objected to because of the following informalities: line 2, "the contact regions" is informal should be --the nitride-based contact region--; and line 6, after "the nitride-based contact", "regions" should be singular --region--.

Claim 79 is objected to because of the following informalities: line 2, "metal allow" (emphasis added) should be --metal alloy--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-45 and 75 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, line 7, "low temperature" is indefinite in scope and meaning as to how low of a temperature is considered as "low".

Re claim 19, line 3, the limitation "the n-type contact layer" lacks antecedent basis and renders the claim unclear in scope and meaning.

Re claim 20, lines 2-3, the limitation "the n-type contact layer" (2 occurrences) lacks antecedent basis and renders the claim unclear in scope and meaning.

Re claim 21, lines 2-3, the limitation "the n-type contact layer" (2 occurrences) lacks antecedent basis and renders the claim unclear in scope and meaning.

Re claim 22, lines 4-5, the limitation "the n-type contact layer" (2 occurrences) lacks antecedent basis and renders the claim unclear in scope and meaning.

Re claim 25, line 10, it is unclear how a “nitride-based” contact region is formed by selectively removing the masking layer and a portion of the contact layer.

Re claim 34, line 2, the limitation "the oxide layer" lacks antecedent basis and renders the claim unclear in scope and meaning.

Re claim 37, lines 1-2, the limitation "the InGaN, GaN ... and/or InN layer" lacks antecedent basis and renders the claim unclear in scope and meaning.

Re claim 45, line 1, the limitation "the contact recess" lacks antecedent basis and renders the claim unclear in scope and meaning.

Re claim 75, lines 2-3, “low temperature” is indefinite in scope and meaning as to how low of a temperature is considered as “low”.

Other claims are rejected as depending on the rejected base claim(s).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7, 8, 13, 16-21, 23, 24, 63-67, 71, 72, 74-76, 79 and 80 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida et al. (U.S. Patent No. 6,534,801).

Re claim 1, Yoshida et al. (“Yoshida”) discloses in FIGs. 1-5 a method of fabricating a transistor, comprising: forming a nitride-based channel layer 3 on a substrate 1; forming a barrier layer 4 on the nitride-based channel layer 3; forming a contact recess 4a in the barrier layer 4 to expose a contact region of the nitride-based channel layer 3; forming a contact layer 5 on the

exposed contact region of the nitride-based channel layer 3 using a “low temperature” deposition process; forming an ohmic contact (S or D) on the contact layer 5; and forming a gate contact G disposed on the barrier layer 4 adjacent the ohmic (S or D).

Re claim 7, Yoshida discloses forming the nitride-based contact layer 5 by molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD) [see col. 4, lines 41 to col. 5, lines 15 and 40-45].

Re claim 8, Yoshida discloses the “low temperature” deposition process is a process (MBE or MOCVD) other than mass transport from a wafer on which the transistor is formed. See discussion above regarding claim 7.

Re claim 13, Yoshida expressly discloses in FIG. 4 the contact recess 4a extends into the channel layer 3.

Re claim 16, Yoshida discloses in FIG. 1 forming a (GaN) contact layer 5 on the exposed contact region 5 of the nitride-based channel layer 3 to a thickness (40 nm) inherently “sufficient” to provide a sheet resistivity of less than a sheet resistivity of a two-dimensional electron gas region formed at an interface between the channel layer 3 and the barrier layer 4 [see col. 3, lines 27-50 and col. 5, lines 9-15]. Regardless, the recitation that an element is “sufficient” to perform a given function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense.

Re claims 17 and 18, Yoshida discloses forming a contact layer comprises forming n-type GaN, wherein the GaN layer is doped with silicon [see col. 5, lines 9-15].

Re claim 19, Yoshida expressly discloses in FIG. 4 forming sidewalls of the channel layer 3 to provide an increased surface area interface between the channel layer 3 and the contact layer 5.

Re claim 20, Yoshida expressly discloses in FIG. 1 forming an ohmic contact (S or D) on the n-type contact layer 5 that extends onto a portion of the channel layer 3.

Re claim 21, Yoshida expressly discloses in FIG. 1 forming an ohmic contact (S or D) on the n-type contact layer 5 that terminates before the sidewall of the channel layer 3.

Re claim 23, Yoshida expressly discloses forming a second contact recess in the barrier layer 4 to expose a second contact region of the nitride-based channel layer 3 [see FIG. 4]; forming a contact layer 5 on the exposed second contact region of the nitride-based channel layer 3 using a “low temperature” deposition process (“selective growth”) [see FIG. 5]; forming a second ohmic contact (S or D) on the contact layer 5 [see FIG. 1]; and wherein forming a gate contact comprises forming a gate contact G disposed on the barrier layer 4 between the first and second ohmic contacts (S and D) [see FIG. 1].

Re claim 24, Yoshida expressly discloses in FIGs. 4 and 5 forming a contact recess 4a that exposes a portion of the barrier layer 4 and wherein forming a contact layer comprises forming a contact layer 5 that extends onto the exposed portion of the barrier layer 4.

Re claim 63, Yoshida discloses in FIGs. 1-5 a method of fabricating a high electron mobility transistor, comprising: forming a nitride-based channel layer 3 on a substrate 1; forming a barrier layer 4 on the nitride-based channel layer 3; forming at least one contact recess in the barrier layer 4 that extends into the channel layer 3; forming a contact region 5 on the nitride-based channel layer 3 in the contact recess; forming a gate contact G disposed on the barrier

layer 4; and wherein forming the contact region 5 and forming the nitride-based channel layer 3 include forming the contact region 5 and forming the nitride-based channel layer 3 to include a surface area enlargement structure 4a.

Re claim 64, Yoshida expressly discloses in FIG. 4 a surface area enlargement structure 4a comprises patterning sidewalls of portions of the contact recess that extend into the channel layer 3.

Re claim 65, Yoshida expressly discloses in FIG. 1 forming an ohmic contact (S or D) on the nitride-based contact region 5.

Re claims 66 and 67, Yoshida expressly discloses in FIG. 1 an ohmic contact (S or D) being extended onto (and not in contact with) the channel layer 3 in the area of the sidewalls. At the same time, the ohmic contact (S or D) can also be seen as not extending onto the channel layer 3 in the area of the sidewalls.

Re claim 71, Yoshida discloses the contact region 5 comprises GaN [see col. 3, lines 10-12].

Re claim 72, Yoshida discloses the contact region 5 comprises GaN doped with silicon [see col. 5, lines 9-15].

Re claims 74 and 75, Yoshida discloses forming the nitride-based contact layer 5 by molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD) [see col. 4, lines 41 to col. 5, lines 15 and 40-45]. In addition, Yoshida discloses forming the contact region 5 comprises forming an n-type semiconductor material (GaN) contact region using a “low temperature” deposition process [see col. 5, lines 9-15].

Re claim 76, Yoshida expressly discloses in FIG. 1 forming a first ohmic contact region S; and forming a second ohmic contact D adjacent the gate contact G and opposite from the first ohmic contact S.

Re claim 79, Yoshida discloses the contact region 5 comprises a metal alloy (GaN) to provide an ohmic contact [see col. 5, lines 9-15].

Re claim 80, Yoshida expressly discloses in FIG. 1 the contact region 5 extending onto the barrier region 4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 5, 6, 15, 77 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Matsumoto et al. (U.S. Patent No. 5,701,019).

Re claims 5, 6, 77 and 78, Yoshida fails to disclose the contact layer comprises an n-type degenerate semiconductor material other than GaN and AlGaN, wherein the contact layer comprises a non-nitride Group III-V semiconductor material, a Group IV semiconductor material and/or a Group II-VI semiconductor material.

Matsumoto et al. (“Matsumoto”) suggests using n-type GaAs (Group III-V semiconductor material) as a contact layer 6, as shown in FIG. 2, for the purpose of decreasing resistance of the contact layer without developing the short-channel effect [see col. 1, lines 35-55].

Since Yoshida and Matsumoto are from the same field of endeavor, the purpose disclosed by Matsumoto would have been recognized in the pertinent prior art of Yoshida.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Yoshida as suggested by Matsumoto because of the desirability to minimize resistance of the contact layer without developing the short-channel effect.

Re claim 15, Yoshida expressly discloses in FIG. 1 forming an ohmic contact comprises patterning a metal layer (to form S, G and D). However, Yoshida does not disclose annealing the patterned metal layer at a temperature of about 850°C or less.

Matsumoto teaches annealing the patterned metal layer (7 and 8) at a temperature of 400°C for the purpose of forming alloys between the contact layer 6 and the patterned metal (7 and 8) [see col. 5, lines 53-60].

Since Yoshida and Matsumoto are from the same field of endeavor, the purpose disclosed by Matsumoto would have been recognized in the pertinent prior art of Yoshida.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Yoshida as taught by Matsumoto because of the desirability to form alloys between the contact layer and the patterned metal. Furthermore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select an appropriate process temperature. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. “Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art … such ranges are termed ‘critical ranges’ and the applicant has the burden of proving such criticality … More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation”. *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Claim 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Vaudo et al. (U.S. Patent No. 6,533,874).

Re claims 2-4, Yoshida fails to disclose the low temperature process uses a temperature of less than 960°C, 450°C or 200°C.

Vaudo et al. (“Vaudo”) mentions forming a GaN layer using a “low temperature” of 100-400°C for the purpose of forming an amorphous GaN nucleation layer [see col. 4, lines 22-27].

Since Yoshida and Vaudo are from the same field of endeavor, the purpose disclosed by Vaudo would have been recognized in the pertinent prior art of Yoshida.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Yoshida as taught by Vaudo because of the desirability to form an amorphous GaN nucleation layer.

Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Nakano et al. (U.S. Patent No. 5,698,870).

Re claim 73, Yoshida fails to disclose forming a silicon nitride layer on the barrier layer and wherein the gate contact is provided in a recess in the silicon nitride layer.

Nakano et al. (“Nakano”) expressly teaches in Figs. 3e-3m forming a silicon nitride layer 328 on a barrier layer 306 and wherein a gate contact (see Fig. 3m) is provided in a recess in the silicon nitride layer 328.

Since Yoshida and Nakano are from the same field of endeavor, the purpose disclosed by Nakano would have been recognized in the pertinent prior art of Yoshida.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Yoshida as taught by Nakano because of the desirability to selectively form a gate contact on the barrier layer.

Claims 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Redwing et al. (U.S. Patent No. 6,727,531).

Re claims 69 and 70, Yoshida discloses using silicon-doped GaN, instead of AlGaN or InGaN, InAlGaN, InAlN and/or InN layer, as the material for forming the contact region.

Redwing et al. (“Redwing”) teaches that silicon-doped GaN, AlGaN or InGaN are equivalent materials known in the art for forming a contact region (“donor layer”) in an HEMT structure [see col. 3, line 60 to col. 5, line 15].

Since Yoshida and Redwing are from the same field of endeavor, the purpose disclosed by Redwing would have been recognized in the pertinent prior art of Yoshida.

Therefore, because these materials were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute GaN for AlGaN or InGaN.

Allowable Subject Matter

Claims 9-12 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

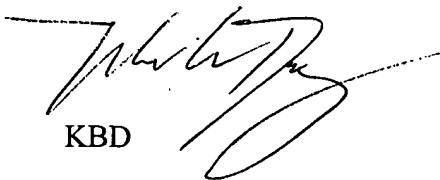
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fareed '809, Huang '386 and Yoshida '101 disclose relevant teachings regarding HEMTs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



KBD



Mary Wilczewski
Primary Examiner